Laboratoire d'Architecture des Processeurs
IN-F Ecublens
CH-1015 Lausanne
http://lapwww.epfl.ch/

Diploma Project
Winter 2003

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

USB 2.0 Development System

Baumann Damien **Computer Science**

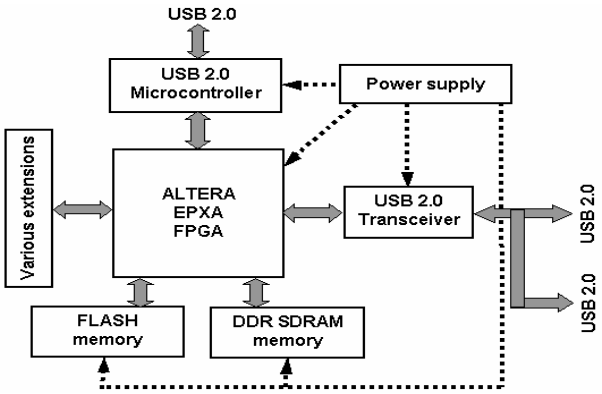
Introduction

A USB 1.1 IP core in VHDL was developed by the candidate during his last semester project. It was implemented on a general card, *AnalysUSB2.0*, designed by P. Musy (E2001) and based on an *Altera 20K100* FPGA, a USB 1.1 microcontroller and a USB 1.1 transceiver. The goal of this project is to create a USB 2.0 development system consisting of a general card, *EPXA4-USB2*, a USB 2.0 IP core in VHDL and a USB 2.0 analyser.

EPXA4-USB2 Development Board

The *EPXA4-USB2* board should be generic enough to be used for complex designs requiring a high density FPGA, USB 2.0 features, embedded processors and large memories. It has the following features:

- Altera *EPXA* containing an *ASIC ARM922T* 32-bit processor with a FPGA of about 400'000 gates
- USB 2.0 microcontroller, *FX2* of *Cypress*
- USB 2.0 transceiver, *ISP1501* of *Philips*
- 128 Mb DDR SDRAM and 16 Mb Flash memory
- Integrated switching power supply
- Various extensions : *Ethernet*, *CompactFlash*, *Milli-Bus*, *Mubus,* 32-bit acquisition channel, *RS232*, *JTAG*, etc.



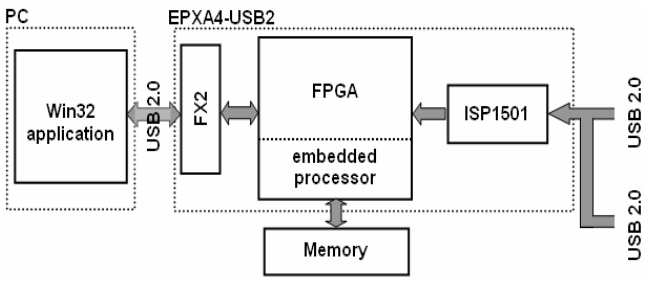
In addition, two extension cards, one for *ISP1501* and one for *FX2,* were developed for the *Altera*'s *Excalibur NIOS* development board in order to provide USB 2.0 functionalities.

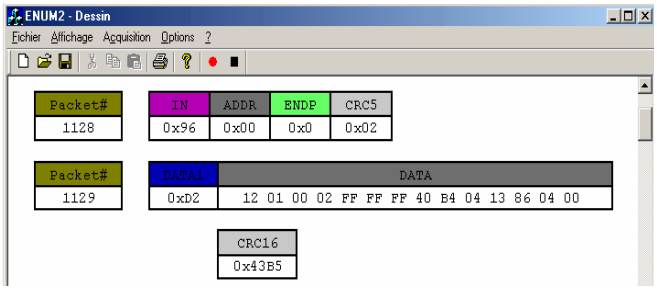
USB 2.0 Microcontroller on FPGA

This module is composed of a USB 2.0 IP core and an embedded processor, for example *ARM* or *Altera softcore NIOS*. The developed USB IP core is relatively independent from the processor and is a useful piece of IP which could be used in other FPGA or ASIC designs. This module is able to run in high-speed of full-speed mode. This design will be placed on the *EPXA4-USB2's* FPGA. In addition, a small *Win32* application will be realised to ensure the smooth running of the system. It will communicate with a PC using the C library previously developed by the *HES-SO.*

USB 2.0 Analyser

This analyser provides a hardware and software system for observing the traffic, in high-speed or full-speed mode, on a USB 2.0 transmission. The hardware part is implemented on the *EPXA4-USB2* board. The USB packets are transmitted to a PC using the USB 2.0 protocol. In addition, a *Win32* application displays the USB transactions and gives the possibilities for starting, finishing, saving and printing acquisitions.





Future Considerations

This project can impact a lot of possible future developments. Here are some examples:

- Creation of various designs on *EPXA4-USB2* using embedded processors (an *ARM* and one or many *NIOS*)
- Conception of USB 2.0 hardware and/or software applications using *FX2*, *ISP1501*, VHDL IP Core and C library
- Development of a 10 Mb/s *Ethernet* controller
- Development of a *CompactFlash* controller. FPGA would then access *CF* cards as hard disks
- Design of extension cards connected to the *Milli-Bus* extension of *EPXA4-USB2*